[This question paper contains 8 printed pages.]

Your Roll No.....

Sr. No. of Question Paper : 5650 **E**

Unique Paper Code : 42344403

Name of the Paper : Computer System Architecture

Name of the Course : **B.Sc. (Prog) / Mathematical Science**

Semester : IV

Duration : 3 Hours Maximum Marks : 75

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. Question No. **1** is compulsory.
3. Attempt any **5** of questions Nos. **2** to **9**.
4. Parts of a question must be answered together.

1. (a) Write the characteristic table of SR flip-flop. (2)

(b) Perform the following operations using signed-2's complement notation for negative numbers in 8-bit representation :

P.T.O.

(i) +42 + (–13)

(ii) –42 – (–13)

(2)

(c) Convert the following numbers to the indicated bases : (2)

(i) $(12121)_3$ to $(----)_{10}$

(ii) $(A675)_{16}$ to $(----)_8$

(d) Differentiate between selective-set and selective-clear. (2)

(e) What is Register? State the use of PC. (2)

(f) Consider the given micro-operation : (2)

$M[AR] \leftarrow AC,\ SC \leftarrow 0$

Write the name of given instruction and state its function.

(g) What is cycle stealing in DMA? (2)

(h) Draw the truth table and logic diagram of Half-Adder. (2)

(i) Specify the output of the following micro-operation : (2)

$R3 \leftarrow R1 + (R2)' \leftarrow 1$

(j) Expand the following terms : (2)

(i) CMOS

(ii) ASCII

(iii) TTL

(iv) ECL

(k) Write micro-operations for a following instruction in the basic computer : (2)

LDA (Load to AC)

(l) Construct an 8-to-1 -line multiplexer with two 4-to-1-line multiplexers and one 2 to-1-line multiplexer. Use block diagrams for the three multiplexers. (3)

2. (a) Simplify the following function in Sum-Of-Products (SOP) form using K-map. Also draw the logic diagram.

P.T.O.

$F(P, Q, R, S) = \Sigma(0, 2, 5, 7, 8, 10, 11, 12, 14)$

$d(P, Q, R, S) = \Sigma(4, 6)$ (6)

(b) Given the following Boolean function : (4)

$F = A'B + ABC' + ABC$

(i) Simplify the given function F using Boolean algebra.

(ii) Find complement of F using DeMorgan's theorem.

3. (a) A two-word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W + 1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is

(i) direct

(ii) indirect

(iii) indexed (6)

(b) Draw the logic diagram of a 2-to-4-line Decoder with only NOR gates including an enable input. (4)

4. (a) Design a combinational circuit with three inputs a, b, c and three outputs P, Q, R. When the binary input is 0, 1, 2 or 3, the binary output is one greater than the input; otherwise, the binary output is one less than the input. (6)

(b) Obtain the 9's complement of the following 8-digit decimal numbers :

(i) 90009951

(ii) 12349876 (2+2)

5. (a) Explain the functioning of a DMA Controller with the help of a block diagram. (6)

(b) A computer has 32-bit instructions and 12-bit addresses. If there are 250 two-address instructions, how many one-address instructions can be formulated? (4)

6. (a) What is the use of Binary Counter? Draw the 4-bit synchronous binary counter. (2+4)

(b) What is Programmed I/O? Specify any one method that can avoid the drawback of programmed I/O. (4)

7. (a) Design a 4-bit Binary Adder-Subtractor circuit diagram using full-adders. (6)

(b) Consider the following Registers with given values :

$R1 = (00110101)_2$

$R2 = (01100111)_2$

$R3 = (10111001)_2$

$R4 = (11101010)_2$

Determine the 8-bit binary representation of values in each register after the execution of the following sequence of operations. Perform the following operations using R1, R2, R3 and/or R4.

(i) $R1 \leftarrow R1 \oplus R2$

(ii) $R3 \leftarrow R4 - R3$ (4)

8. (a) A computer uses a memory unit with 512K words of 3 2 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. (6)

(i) How many bits are there in the operation code, the register code part, and the address part?

(ii) Draw the instruction word format and indicate the number of bits in each part.

(iii) How many bits are there in the data and address inputs of the memory?

(b) List the micro-operations for Fetch and Decode Phase of Instruction Cycle. (4)

9. (a) Draw the block diagram for the hardware that implements the following :

$$x + yz : AR \leftarrow AR + BR$$

where AR and BR are two n-bit registers and x, y and z are the control variables. Include the logic gates for the control function. (6)

P.T.O.

(b) Write a program to evaluate the arithmetic statement :

$$X = (A+B) * (C+D)$$

using two address and three address instructions. (4)